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A 1.5V Area Efficient Asynchronous Adder using MODL and Double Pass Transistor Logic

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Abstract— The increasing demand for low power VLSI can be fulfilled to a great extend by making proper changes in the circuit level and architectural level design. Addition is a fundamental operation, as it is used to implement more complex functions such as subtraction, multiplication, division etc. The Manchester Carry Chain adder design is preferred to other adders, regardless the number of bits because of its high-speed and is wide applications. A new technique is presented in this paper for the implementation of a 32 bit Adder which operates at low power. Even though this implementation is structurally inherited from Manchester Carry Chain based Adder, it is highly area efficient without much increase in delay. The proposed adder was based on Multiple Output Domino logic, which helps to reduce the complexity of the adder implemented using Manchester Carry Chain adder implemented in CMOS logic. At the same time, the 4T implementations of XOR based circuits in the adder design results in lesser number of transistors for its implementation and thereby provide a low power/size solution for arithmetic functions. The simulation result shows a reduction of 25% in size, over CMOS adder implemented using the same Manchester Carry Chain topology at 1.5v Supply voltage with the help of TSMC .18u technology.

Index Terms—Adder, Asynchronous Circuits, Manchester Carry Chain, Low Power, Domino Pass transistor Logic, XOR, Carry Look-Ahead Adder,.

1 INTRODUCTION

THE demand for low power Very large Scale Integration is increasing day by day at different levels such as process technology level, architectural, circuit and layout. By proper selection of logic style for the implementation of functions, a considerable amount of power saving can be done in its implementation. Addition [1], [4] is a fundamental operation as it is used to implement more complex functions such as subtraction, division, multiplication, etc. The advantages for carry look-ahead over other adder design are its ease of design and high speed. Among all carry look-ahead circuits, Manchester carry chain based adder circuit has the smallest transistor count. The Manchester carry chain generate the carry signals by processing signals from the carry generate and propagate blocks.

A Manchester carry chain circuit implemented in CMOS PTL logic is shown in Fig. 1 which has been used to implement arithmetic functions. The function of the Manchester carry chain circuit is: Ck = Gk+Ck-1.Pk for k = 1 to n, where n is the bit number, Gk and Pk are the generate and propagate signals produced from two inputs of the half adder.

Domino logic gates are used to cascade CMOS dynamic gates, since dynamic gate's finite pull down time for output node to start its discharge. Pass transistor Logic (PTL) [4] has the advantage of being fast, and complex logic gates can be implemented with minimal number of transistors. Power consumption and circuit performance of PTL based circuits vary. However, the nMOS pass transistor does not transmit good "1" and pMOS pass transistor cannot pass a good "0". Hence level restorers may be required at the output of logic gates.

For the implementation of sum circuits, and carry generate signals, XOR function is essential and therefore the count of the transistors used for XOR implementation will reflect the size of the adder. Normal implementation of XOR function ie; the mirror circuit implementation of XOR, in which the NMOS and P-MOS arrays have the exactly the same structure uses 8 transistors.

PTL logic preliminaries are given in section II. The rest of the paper is as follows: Conventional Manchester Adder in section III. Next, the description of our proposed area efficient adder is given in section IV. The comparative results based on our proposed approach using Mentor Graphics ELDO Spice are given in section V.

2 MULTIPLE OUTPUT DOMINO LOGIC

Domino Logic gates are used to cascade CMOS dynamic gates, since its high pull down time for output node to start its discharge. Cascading similar stages at the output is done with the help of inverter at the output stage. Fig. 1 shows the cascading of two stages in CMOS domino logic [7],[8]. The operating period of a cell when its input clock and output are low is called the pre charge phase. The next phase, when the clock is high, it is called evaluate phase.

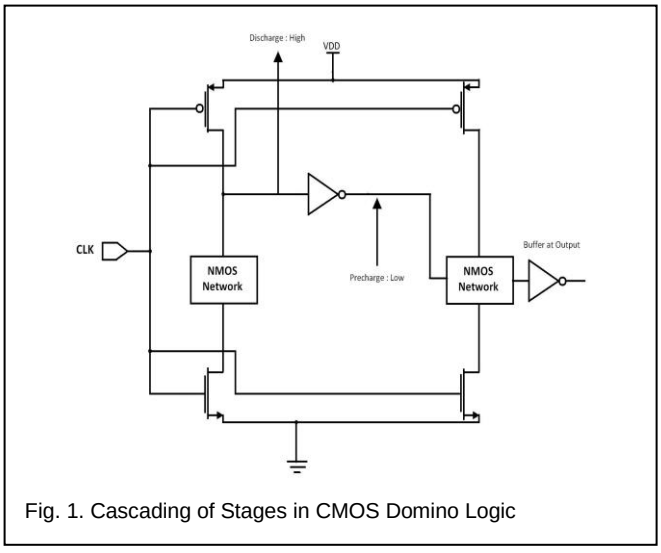


Fig. 1. Cascading of Stages in CMOS Domino Logic

When the clock is low, dynamic node is pre charged to high and the output of the first buffer will become low. nMOS present in the next logic block will be in OFF condition. When the clock goes to HIGH, dynamic node is conditionally discharged and the output at the buffer will simultaneously go to HIGH

state. Buffer output can only make one Low to High transition because dynamic discharge can only happen once[9].

When domino gates are cascaded and if the output of each stage rises, it will evaluates and that results in triggering the evaluation of the next stage till the last stage in the cascaded structures like a line of dominos falling[10]. Similarly, once the internal node in a gate falls, it will stay in the same state, until it is picked up by the precharge phase of the next cycle.

In Fig. 2 the pMOS keeps dynamic node at logic '1' during evaluation phase, even though it is pulled down by the nMOS network. Here the pMOS is On for all the time and hence the power dissipation will be more compared to CMOS[10].

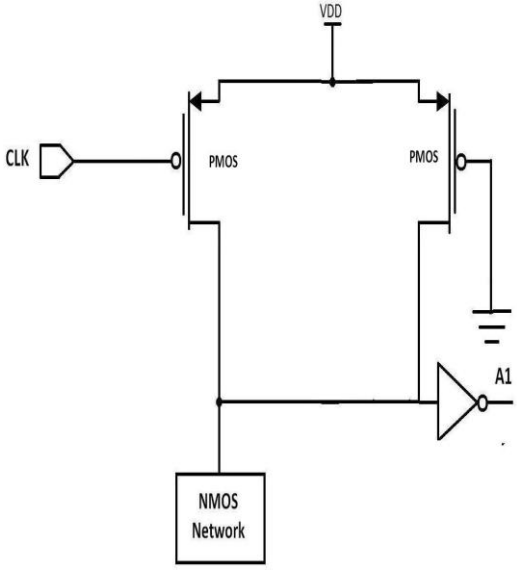


Fig. 2. Domino logic Circuit

3 CONVENTIONAL MANCHESTER ADDER

A carry look ahead adder is a type of adder used in digital logic. A carry look ahead adder improves speed by reducing the amount of time required to determine carry bits compared to simple ripple carry adder in which the carry bit is calculated along with the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits The carry look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the next value bits.

The equation for the sum of a 4 bit Manchester carry adder will be as follows.

1. S0 = A0 XOR B0 XOR Cin
2. S1 = A1 XOR B1 XOR C0
3. S2 = A2 XOR B2 XOR C1
4. S3 = A3 XOR B3 XOR C2

The equation for the carry and carry generate and propagate of a 4 bit Manchester carry adder will be as follows.

1. Carry_out = C3
2. Ck = Gk + Ck-1.Pk for k = 1 to n
3. Gk = Ak XOR Bk
4. Pk = Ak.Bk

The circuit diagram of AND block in CMOS logic is as follows.

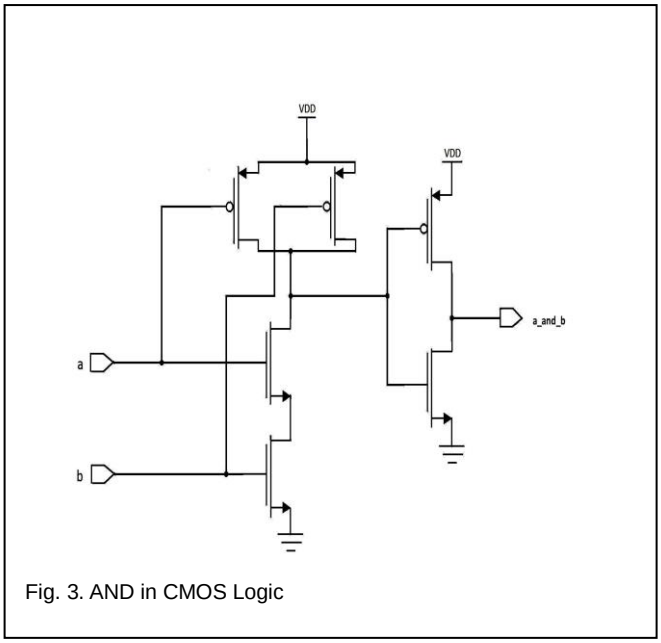


Fig. 3. AND in CMOS Logic

The circuit diagram of the Manchester carry Chain and XOR implementation of 4 bit conventional adder is shown in the Fig:3 and Fig:4 . It uses a total of 27 transistors for implementing Manchester carry chain and 8 transistors for implementing the XOR [3] function.

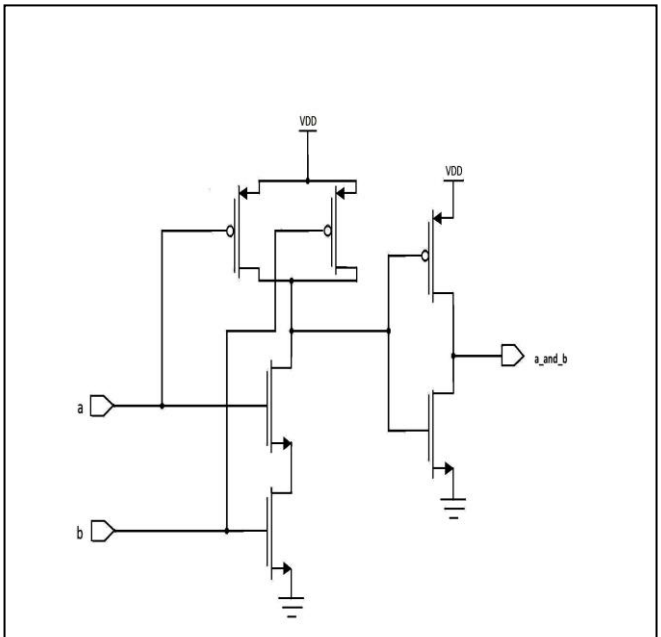


Fig. 4. AND in CMOS Logic

2 PROPOSED AREA EFFICIENT ADDER

The proposed PTL quad bit adder was based on the following energy saving rules [2] and the rules are as follows.

1. The use of precharged dynamic logic, results in minimization of total charge deposited during precharge, since the change in input signal should gate the transistor that is nearest to the precharged output node.

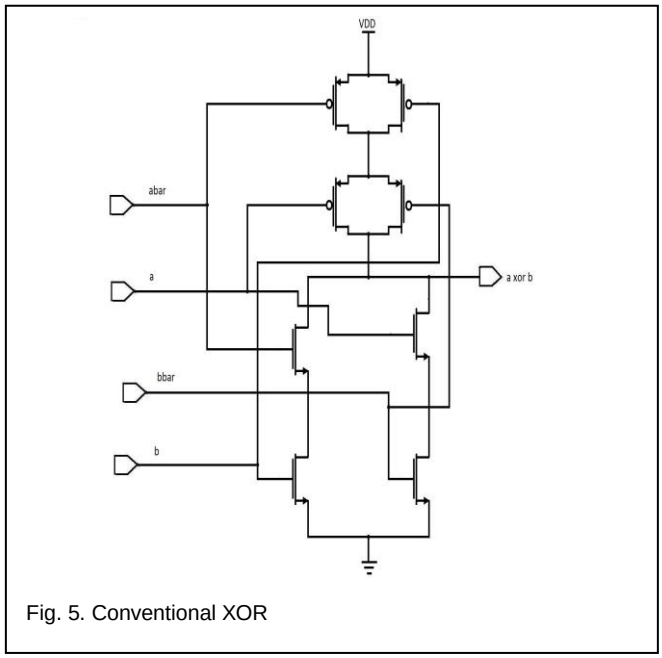


Fig. 5. Conventional XOR

2. PTL implementation of XOR gate results in use of less number of transistors, in turn results in less energy consumption for arithmetic functions which contains XOR gates.

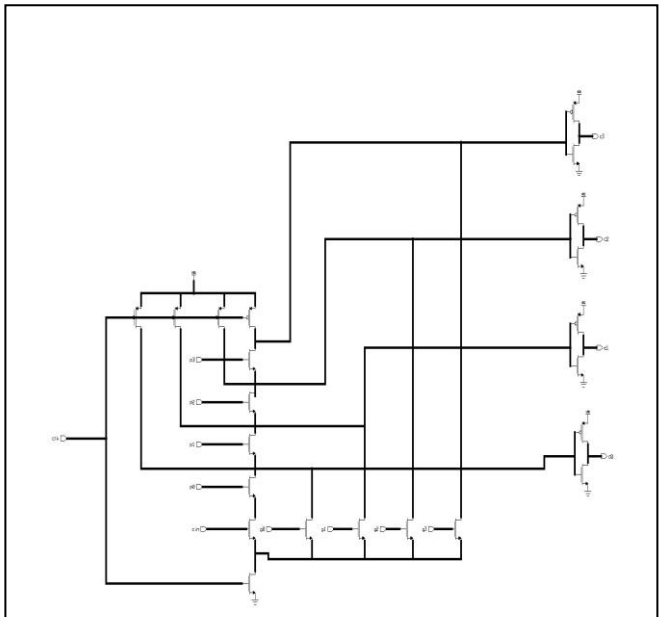
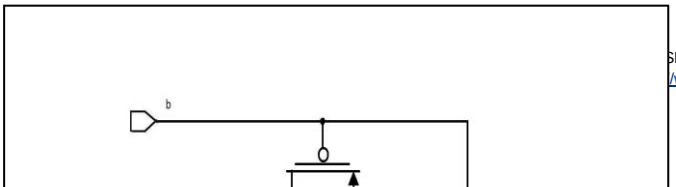


Fig. 6. Carry Chain of Proposed Adder



The Fig. 5, Fig. 6, circuit diagram of the Manchester carry Chain and XOR of the proposed area efficient adder. Here it uses only 22 transistors for implementing Manchester carry chain and 6 transistors for XOR implementation. Thus it shows a reduction of 25% in transistor count compared to the Conventional Manchester adder. The Block representation of the proposed 32 bit adder was shown in Fig.8.

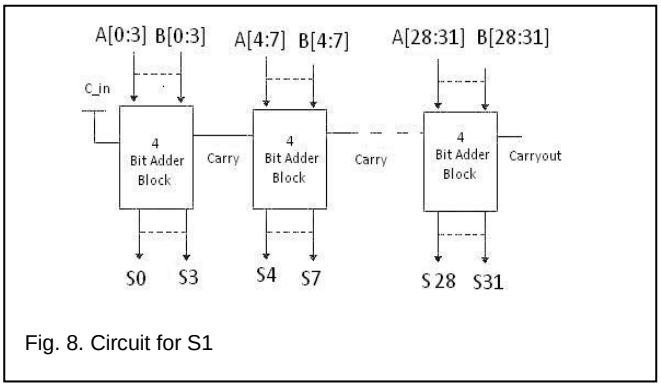


Fig. 8. Circuit for S1

5 CONCLUSION

In the proposed design a 32 bit adder was implemented using modified Manchester chain and 4T XOR implementation in ripple carry topology. The proposed design is much more area efficient compared to implementation of 32 bit adder in conventional Manchester chain and XOR design style. The proposed 32 bit adder was shown in Fig. 7. The proposed 32 bit adder uses a total number of 880 transistors where as the conventional implementation requires 1176 transistors. Thus the result shows a reduction of 25% in size. The reduction in number of transistor results in considerable reduction power

consumption. The schematic entry was done using mentor graphics Design architect and simulation was done using Mentor Graphics ELDO. The following parameters are used for simulation. Wpmos = 240nm; Wnmos = 360nm. The simulation was done using TSMC 180nm process technology at 1.5v.

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